AMENDMENTS TO THE CLAIMS

Claims 1-63. (Cancelled)

64. (Original) A capacitor structure formed by the method comprising:

forming a container opening in a first insulating layer formed over a substrate;

forming an oxide layer over said substrate;

forming a plug over said oxide layer;

forming a second insulating layer over said plug and said first insulating layer;

etching said second insulating layer such that the space formed in said second insulating layer is wider than said plug;

removing said plug and said oxide layer to form a container opening;

forming a first conductive layer in said container opening over an active area of said substrate;

forming a first dielectric layer atop said first conductive layer; and

forming a second conductive layer atop said dielectric layer.

65. (Original) The capacitor structure according to claim 64, wherein said capacitor is a container capacitor.

66. (Original) The capacitor structure according to claim 64, wherein said first conductive layer and second conductive layer are independently formed of a material selected from doped polysilicon, hemispherical grained polysilicon or a metal.

67. (Original) The capacitor structure according to claim 66, wherein said first conductive layer is formed of hemispherical grained polysilicon.

68. (Original) The capacitor structure according to claim 66, wherein said second conductive layer is formed of doped polysilicon.

69. (Original) The capacitor structure according to claim 64, wherein said dielectric layer is selected from the group consisting of oxides and nitrides.

70. (Original) The capacitor structure according to claim 69, wherein said dielectric layer is selected from the group consisting of Ta_2O_5, $SrTiO_3$, Y_2O_3, Nb_2O_5, ZrO_2, titanium oxide, and silicon nitride.

71. (Original) The capacitor structure according to claim 64, wherein said capacitor is a stacked capacitor.

72. (Original) The capacitor structure according to claim 64, wherein said first conductive layer is in direct contact with an active area in said substrate.

73. (Original) The capacitor structure according to claim 64, wherein said integrated circuit is a DRAM cell.

Claims 74-81. (Cancelled)